REMARKS

Claims 10, 12, 17 and 18 are pending. Applicants propose amendment of claims 10, 17 and 18, and cancellation of claim 11. Entry of the proposed amendments after final action is earnestly solicited.

Rejections under 35 USC §112

Claim 11 was rejected under 35 USC §112, second paragraph as being indefinite.

Applicants propose cancellation of claim 11 which would render this rejection moot.

Rejections under 35 USC §102(b)

Claims 10-12, 17 and 18 were rejected under 35 USC §102(b) as being anticipated by Venkatesan et al. (U.S. Patent No. 5, 459, 096). Favorable reconsideration of this rejection is respectfully requested.

Applicants propose amendment of claims 10, 17 and 18 to recite "polishing the first surface and second surface to obtain the front-and-back electrically conductive substrate, wherein the first surface and second surface are electrically connected by the plurality of posts."

Venkatesan et al discloses a process for fabricating a semiconductor device using dual planarization layers. According to Venkatesan et al, the first surface and second surface of the substrate are not polished to obtain the front-and-back electrically conductive substrate. Also,

the first surface and second surface are not electrically connected by the elevated regions 34, which are referred to by the Examiner as the "plurality of posts".

Thus, Venkatesan et al does not teach or suggest "polishing the first surface and second surface to obtain the front-and-back electrically conductive substrate, wherein the first surface and second surface are electrically connected by the plurality of posts," as recited in amended claims 10, 17 and 18.

For at least these reasons, claims 10, 12, 17 and 18 patentably distinguish over Venkatesan et al.

Rejections under 35 USC §103(a)

Claims 10-12, 17 and 18 were rejected under 35 USC §103(a) as being obvious over Venkatesan et al. (U.S. Patent No. 5,916,453) in view of Albrecht et al. (U.S. Patent No. 4,968,585). Favorable reconsideration of this rejection is respectfully requested.

The Examiner alleges that even if Venkatesan et al does not disclose the post being formed by anisotropically etched silicon, Albrechit et al discloses it.

However, as discussed above, Venkatesan et al fails to disclose "polishing the first surface and second surface to obtain the front-and-back electrically conductive substrate, wherein the first surface and second surface are electrically connected by the plurality of posts."

Albrecht et al has been cited for allegedly disclosing anisotropic etching. Such disclosure, however, does not remedy the deficiencies of Venkatesan et al discussed above.

Moreover, nothing in Albrecht et al indicates that the microfabricated cantilever stylus can be related to the front-and-back electrically conductive substrate as recited in the pending claims.

For at least these reasons claims 10, 12, 17 and 18 patentably distinguish over Venkatesan et al and Albrechit et al.

In view of the aforementioned amendments and accompanying remarks, Applicants submit that that the claims, as herein amended, are in condition for allowance. Applicants request such action at an early date.

If the Examiner believes that this application is not now in condition for allowance, the Examiner is requested to contact Applicants' undersigned attorney to arrange for an interview to expedite the disposition of this case.

If this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. The fees for such an extension or any other fees that may be due with respect to this paper may be charged to Deposit Account No. 50-2866.

Respectfully submitted,

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